



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,861	01/14/2004	Andrew A. Charles	1	3400
40984	7590	03/22/2006	EXAMINER	
WERNER ULRICH 434 MAPLE STREET GLEN ELLYN, IL 60137-3826			YU, JAE UN	
			ART UNIT	PAPER NUMBER

2185

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,861	CHARLES, ANDREW A.	
	Examiner	Art Unit	
	Jae U. Yu	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>6/2/2004</u> | 6) <input type="checkbox"/> Other: _____ |

DTAILED ACTION

The instant application having Application No. 10756861 has a total of 20 claims pending in the application, there are 2 independent claims and 18 dependent claims, all of which are ready for examination by the examiner.

Information Disclosure Statement

As required by M.P.E.P. 609 (C), the applicant's submission of the Information Disclosure Statement dated on 6/2/2004 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1, 11, 12, and 16-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
2. Claims 1 and 11 recite the limitation "the adding of said surplus block". There is insufficient antecedent basis for this limitation in the claim.

3. **Claims 11, 12 and 16-18** are means plus function claims, and interpreted according to 35 U.S.C. 112 sixth paragraph. The “means” recited in the claims are not disclosed in the specification in a manner which one skilled in the art would be able to identify the structure from the description in the instant specification for performing the recited function. See MPEP 2181 (III). Accordingly, the limitations are indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. **Claims 1, 6-11 and 16-20** are rejected under 35 U.S.C. 102(b) as being anticipated by Celi Jr. et al. (US 5,742,797).

2. **Independent claims 1 and 11** disclose “method” and “apparatus” for allocating and deallocating memory. **Celi, Jr. et al. disclose the method for allocating and deallocating memory in Figures 5-6, which is stored in a “computer readable media” (Column 10, Line 29) and executed on the system (Figure 2).**

“Assigning to each basic unit of user memory [**Memory blocks, Figure 4A-4D**] a corresponding memory control blocks [**Location entries corresponding to memory blocks, Figure 3**]”

“Collecting groups of contiguous available control blocks into linked lists [**Linked lists of unallocated** (“available” from the claim”) **control blocks, Figure 3**], each list for storing available control block groups having an associated minimum size” **The element 312 of Figure 3 indicates the size of a corresponding user memory block, wherein the list is organized according to region size from smallest available sized region** (“minimum size” from the claim) **to largest (Column 7, Lines 63-67).**

“In response to a request for a block of user memory [**A request for a region of memory, Column 7, Lines 60-61**], searching for a linked list having available blocks of user memory at least as large as the requested size [**Traversing the linked list to locate an unallocated** (“available” from the claim) **region of sufficient size, Column 7-8, Lines 64-6**]”

“Seizing a block of user memory of the required size [**Allocating a memory region of sufficient size for the memory request, Column 7-8, Lines 60-6**] and making available any surplus [**“Unallocated” Region 404, Figure 4A**] representing the difference between the requested size of memory [**“Image #1” 402, Figure 4A**] and the size of the seized block of user memory [**Element 211D, Figure 4A**]”

“When deallocating memory [**Deallocation of a memory region, Column 8, Lines 55-54**], testing whether user blocks of memory [**Element 402, Figure 4C**] immediately

adjacent to the deallocated block **[Element 410, Figure 4C]** are available and if available merging the available blocks to the block being deallocated to create a merged deallocated block” **After the element 402 is deallocated (“available” from the claim), it is merged with the adjacent available block (Element 410) to create a merged deallocated block (Element 412, Figure 4D).**

“Inserting the merged deallocated block into a linked list of available blocks of memory for containing blocks of memory of the size of the merged block” **Celi Jr. et al. disclose, “Recompute the available memory region options and reform the linked list” step 604 in Figure 6, wherein the reforming includes combining contiguous unallocated regions into a single unallocated region (Column 9, Lines 39-43) and updating the linked list (Figure 3) for “Image #1” (Element 402, Figure 4C) according to the size of the merged block (Element 412, Figure 4D).**

“Whereby the adding of said surplus block **[Adding the “Unallocated” Region 404 to a Linked List, Figure 3 and 4A]** and the process of creating a merged deallocated block **[Figure 4C and 4D]** helps to avoid fragmentation of memory **[Element 404 of Figure 4A and Element 412 of Figure 4D are defragmented memory blocks]**”

2. **Claims 6 and 16** disclose, “the step of grouping available block groups **[Unallocated Blocks, Figure 3 & 4]** into two-way linked lists **[“Doubly Linked List”, Column 5, Line 42, Figure 3]**”.

3. **Claims 7 and 17** disclose, “ordering said linked list by size” **[Organizing linked list by size, Column 7, Lines 65-66]**.

“Finding the linked list having a minimum size at least as large as the requested size **[Traversing the linked list from smallest region to largest region to locate a region of sufficient size based on the memory request, Column 7-8, Lines 60-7]**”

“Substantially searching over linked list for blocks of memory larger than the minimum size linked list until a linked list is found having an available block **[“Unallocated Region”, Column 8, Line 4]** of user memory **[Traversing the linked list from smallest region to largest region to locate a region of sufficient size based on the memory request, Column 7-8, Lines 60-7]**”

4. **Claims 8 and 18** disclose, “storing availability bits **[Elements 304, 305, 306 and 307, Figure 3]** for each basic unit of user memory”.

“In case said memory control blocks are inadvertently overwritten **[Updating control blocks (Figure 3 & Step 604 of Figure 6) corresponding to the merged block (Element 412, Figure 4D), recreating a new set of linked lists [Element 604, Figure 6]** from data of said availability bits **[Element 602, Figure 6]**”

5. **Claims 9 and 19** disclose, "the memory control blocks are contiguous to each other [**Control blocks contiguously linked to each other, Figure 3**] and located separately from the user memory [**User memory (Figure 4) located separately on locations specified the control blocks (Element 310, Figure 3)**]".

6. **Claims 10 and 20** disclose, "user memory is in one contiguous block [**Element 404, Figure 4A**] and control memory is in a separate contiguous block [**Element 304, Figure 3**] and wherein addresses of each basic unit of user memory and each control block [**Elements 304, 305, 306 and 307, Figure 3**] are related by a corresponding distance [**Element 312, Figure 3**] from a starting point [**Element 310, Figure 3**] of said user memory and said control block memory [**Element 304, Figure 3**]".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. **Claims 2-5 and 12-15** are rejected under 35 U.S.C. 103(a) as being obvious over Celi Jr. et al. (US 5,742,797) in view of Calderon et al. (US 2003/0225991 A1).

2. As per **claims 2 and 12**, Celi Jr. et al. disclose the method and apparatus recited in claims 1 and 11.

Celi Jr. et al. do not disclose expressly, "providing a linked list for each size that is a multiple of a basic block size".

Calderon et al. disclose a packet-switching system that comprises "a linked list" of packets varying from 1 to 64 bytes, wherein a basic block size can vary from 1 to 64 bytes in paragraphs 16 and 17.

Celi Jr. et al. and Calderon et al. are analogous art because they are from the same field of endeavor of memory access management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Celi Jr. et al. by including a packet-switching system that provides a linked list for blocks varying from 1 to 64 bytes as taught by Calderon et al. in paragraphs 16 and 17.

The motivation for doing so would have been the benefits of increasing memory access efficiency as expressly taught by Calderon et al. in paragraph 46.

Therefore, it would have been obvious to combine Calderon et al. with Celi Jr. et al. for the benefit of increasing memory access efficiency to obtain the invention as specified in claims 2 and 12.

3. **Claims 3 and 13** disclose, "said basic block size is 64 bytes [**A 64 bytes packet, Paragraph 16**"]".

4. **Claims 4 and 14** disclose, "lists are provided for each block size [**"a linked list" of packets varying from 1 to 64 bytes, Paragraphs 16 & 17**] that is a multiple of a basic block size [**Basic blocks varying from 1 to 64 bytes, Paragraph 16**] up to some limit [**"Maximum Packet Size", Paragraph 16**] and wherein block sizes above said limit are in multiples of a superblock size, said superblock size being larger than said basic block size [**Any block sizes between 1 byte to 4 megabytes larger than the "basic block size", Paragraph 16**]".

5. **Claims 5 and 15** disclose, "said superblock size is 4K bytes [**Block sizes between 1 byte to 4 megabytes, Paragraph 16**]".

Relevant Art Cited by the Examiner

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See MPEP 707.05 (C).

The following reference teaches **dynamic memory allocation using a tree structure**.

U.S. PATENT UNNUMBER

5,742,793

FIGURES

3-5

Conclusion

A. Claims Rejected in the Application

Per the instant office action, claims 1-20 have received a first action on the merits and are subject of a first action non-final.

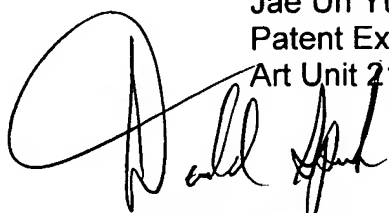
B. Direction of Future Correspondences

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae U. Yu whose telephone number is 571-272-1133. The examiner can normally be reached on M-F 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 15, 2006

Jae Un Yu
Patent Examiner
Art Unit 2185

DONALD SPARKS
SUPERVISORY PATENT EXAMINER